⑲日本国特許庁（ＪＰ）　⑪特許出願公開

⑫公開特許公報（Ａ）　平4-155834

⑸Int.Cl.⁵　識別記号　庁内整理番号　㊸公開　平成４年(1992)５月28日
H 01 L 21/3205
21/31
21/90　M　7353-4M
7353-4M　H 01 L 21/88　D
7342-4M　21/95
審査請求　未請求　請求項の数　２　（全５頁）

㊹発明の名称　多層層間絶縁膜のエツチング方法

㉑特　願　平2-281469
㉒出　願　平２(1990)10月18日

㉒発明者　斎藤　雅彦　大阪府大阪市阿倍野区長池町22番22号　シャープ株式会社内
㉑出願人　シャープ株式会社　大阪府大阪市阿倍野区長池町22番22号
㉔代理人　弁理士　梅田　勝　外２名

明　細　書

1．発明の名称

多層層間絶縁膜のエッチング方法

2．特許請求の範囲

1）多層配線間を電気的に分離する絶縁膜にスルーホールを形成する方法において、

下層配線が形成された半導体基板上にＳｉＮ膜及び有機膜を含む複合絶縁膜を形成し、

O_2を含む雰囲気中でのドライエッチングにより上記有機膜に開口を形成し、

上記有機膜をマスクに、CHF_3とO_2の混合ガス雰囲気中でＳｉＮ膜に異方性エッチングにより開口を形成し、

上記ＳｉＮ膜のエッチング条件よりO_2濃度を高く設定したCHF_3とO_2の混合ガス雰囲気中で上記複合絶縁膜の開口壁を後退させる工程とにより、スルーホールを形成することを特徴とする多層層間絶縁膜のエッチング方法。

2）請求の範囲第１項の記載において、有機膜はポリイミド膜であり、ポリイミド膜を異方性エッチングするためのCHF_3とO_2混合ガスのO_2の濃度は、ほぼ１０～３０％に設定されてなることを特徴とする多層層間絶縁膜のエッチング方法。

3．発明の詳細な説明

＜産業上の利用分野＞

本発明は半導体装置の製造方法に関し、特には多層配線の上層配線と下層配線を互いに接続するスルーホールの形成に関する。

＜従来の技術＞

一般に半導体装置が高密度化するのに伴って、電極配線の多層化，パターン幅の微細化が要求されている。

このような状況に対応するため、多層層間絶縁膜の形成方法も多様化している。この種の絶縁膜としては、プロセス（平坦化，微細化）又はデバイス特性上、複数種類の絶縁膜を積層した複合膜を用いることが多い。例えば最近のデバイスとしては、層間絶縁膜にプラズマＣＶＤ法で形成したＰ－ＳｉＮ膜と、ポリイミド膜を重ねて２層構造にしたものが多く用いられている。この種の複合

膜の主な特徴として、（１）Ｐ－ＳｉＮ膜を下層に用いることにより、ポリイミド膜の吸湿による水分及び膜中の不純物がシリコン基板に到達することを防ぐことができる。（２）ポリイミド膜の分極によるシリコン基板の表面反転や，ＭＯＳトランジスタのスレッシュホールド電圧を変化させるという悪影響をＰ－ＳｉＮ膜によって減少できる。（３）Ｐ－ＳｉＮ膜の段差被覆性の悪さ，クラック発生等を上層のポリイミド膜により平坦化し、層間絶縁膜としての信頼性をより完全なものにすることができる、等が挙げられる。

このような積層した複合膜に対するスルーホールの形成方法については、上層のポリイミド膜はウエットエッチング（ヒドラジン液，アルカリ現像液），ドライエッチング，感光性ポリイミドの利用等により開口を形成している。

一方、下層のＰ－ＳｉＮ膜についてはドライエッチング処理により開口を形成しているが、上記複合膜にエッチングを施すと、ポリイミド膜とＰ－ＳｉＮ膜の境界においてＰ－ＳｉＮ膜に対しポリイミド膜がオーバーハング構造になり易い。第２図にオーバーハング構造の例を示す。

同図において、下層配線１上に積層されたＰ－ＳｉＮ膜２及びポリイミド膜３は、ホトレジスト４をマスクとして開口が形成されているが、Ｐ－ＳｉＮ膜２の開口面積が、ポリイミド膜３の開口面積に比べて大きくなっており、オーバーハング構造を呈する。

このような場合、開口部に上層配線５を被着すると、第３図のように突出したポリイミド膜２のために陰になる部分が生じ、段差被覆性が著しく悪くなり、断線する場合もある。そのため第４図に示すように、上層のポリイミド膜３をエッチング後、下層のＰ－ＳｉＮ膜２を異方性エッチングするか、第５図に示すような、下層のＰ－ＳｉＮ膜２の開口面積をポリイミド膜３のそれより小さくするために、Ｐ－ＳｉＮ膜２上をマスク材料で被って一旦開口を形成し、マスク材料４を除去した後、その上に上層のポリイミド膜２を被って開口を形成するといった、それぞれにマスク材料を形成し、エッチングするか、オーバーハング構造を防止するために、ポリイミド膜３，Ｐ－ＳｉＮ膜２のエッチング後、上層のポリイミド膜３のみを更にエッチングするか、第６図に示すように、マスク材料４のテーパー角と、マスク材料４とポリイミド膜３との選択比（エッチング速度比）によって上層のポリイミド膜３のテーパー角を制御し、更に上層のポリイミド膜３のテーパー角と、上層のポリイミド膜３及び下層のＰ－ＳｉＮ膜２の選択比により下層のＰ－ＳｉＮ膜のテーパー角を制御して、段差被覆性の優れた開口を、ＲＩＥにより形成すること等により対処してきた。

＜発明が解決しようとする問題点＞

上記従来のプロセスにおいて、第４図に示すように、下層Ｐ－ＳｉＮ膜２を異方性エッチングする方法は、異方性が完全であったり、異方性を達成しても、近年の微細化に伴う開口部のアスペクト比（開口部の幅に対する深さの比）の上昇により、配線材料の段差被覆性が悪くなる。

第５図に示すように、２度に分けてマスクを形成し、エッチングする方法は、工程が複雑である、マスク形成の際に合わせ精度が要求される、及び開口部の寸法が拡大する。またマスク形成の際にズレを生じていると実際の開口部の寸法が小さくなり過ぎ、導通が確保できなくなる場合も生じる。更に、一旦開口を形成した後上層のポリイミド膜３のみをエッチングし、オーバーハング構造を防止する方法は、下層のＰ－ＳｉＮ膜２のオーバーハング状態に左右される。このため上層のポリイミド膜３のみの後退量を充分にとる必要があり、開口の寸法が拡大する。

また第６図に示すように、マスク材料４及び上層ポリイミド膜３のテーパー角と、マスク材料と絶縁膜及び絶縁膜同士の選択比により開口部のテーパー角を制御する方法は、エッチング面積比の変化、絶縁膜自身の膜質の変化により、テーパー角の制御性が悪くなる。

また最初からテーパー角を考慮したエッチングを行っているため、オーバーエッチングに対して後退量が大きくなり、開口部の寸法が拡大する。

更に最適エッチングまでは、良好なテーパーが形成できても、オーバーエッチングにより結局垂直形状になってしまう等、不安定要因が多い。

本発明は上記従来方法の問題点に鑑みてなされたもので、開口寸法の微細化と配線材料の段差被覆性を満足させるエッチング方法を提供する。

＜問題点を解決するための手段＞

上層下層配線間に、異なる種類の層間絶縁膜を複数層積層してなる半導体装置の、上層下層配線間を接続するためのスルーホールを形成する方法において、上層のポリイミド膜をエッチングした後、下層Ｐ－ＳｉＮ膜をCHF_3とO_2の混合ガスで異方性エッチングし、続いてCHF_3とO_2の混合ガスにおいてＰ－ＳｉＮ膜とは異なるエッチング条件で、ポリイミド膜の開口側壁面とＰ－ＳｉＮ膜の開口上端を同時に後退させ、テーパーをもつスルーホールを形成する。

＜実施例＞

第１図（ａ）～（ｆ）は、本発明の１実施例を説明するための半導体基板の断面図で、特に２層に積層した絶縁膜上をホトレジストで被った後、マスク材料のパターニング工程からエッチング工程及び配線材料の被着工程を示す。

第１図（ａ）において、下層配線１上にプラズマＣＶＤ技術により、Ｐ－ＳｉＮ膜２を形成し、続いてその上にポリイミド膜３を形成し、２層の複合層間絶縁膜とする。次に上記複合層間絶縁膜の所望の位置に開口を形成するために、上層絶縁膜３上にホトレジスト４を塗布し、これに所定のパターンを形成する。ここでホトレジスト４のテーパー角は露光，現像及びベーク条件等を選択することにより、約８０度に設定した。

次に第１図（ｂ）に示すように、ホトレジストの開口部に露出したポリイミド膜３をエッチングするために、まずポリイミド膜３をO_2を主体とするリアクティブイオンエッチング（ＲＩＥ）により開口を形成する。続いて第１図（ｃ）に示すように、Ｐ－ＳｉＮ膜２をCHF_3とO_2の混合ガスを用いて、平行平板型ドライエッチング装置により異方性エッチングする。ここでエッチングの条件は、第７図から第９図に示す実験結果に基づいて設定した条件で実施する。即ち、上記Ｐ－ＳｉＮ膜２の完全異方性形状を得る条件としては、CHF_3とO_2の混合ガスについて、O_2の混合割合を１０～３０％（第７図）望ましくは約２０％，ガス圧をほぼ０．０３～０．１Torr（第８図），高周波電力密度を０．２ｗ／cm^2以上（第９図）に設定する。上記異方性エッチングの条件に設定することにより、ほぼ垂直な側壁をもつ良好なエッチング形状が得られた。なおＰ－ＳｉＮ膜２の膜質によってエッチング速度に変化は見られるが、形状については非常に安定しており、またエッチング後更にオーバーエッチングを最大５０％まで行ったがオーバーハング構造にはならないことが確かめられ、製造時の工程管理が行ないやすくなる。

続いて上記Ｐ－ＳｉＮ膜２に完全異方性エッチングがされた半導体基板に、第１図（ｄ）に示すように、再びCHF_3とO_2の混合ガスを用いてエッチングする。ただし、この工程では微細化を損なうことなく被覆性を高めるために、エッチング条件は上記完全異方性エッチングとは異なる条件に設定する。即ちO_2の混合割合はほぼ５０％（第７図），ガス圧は０．０５Torr（第８図），高周波電力密度は０．２ｗ／cm^2以上（第９図）としてエッチングする。上記エッチング条件で行うことにより、ポリイミド膜３の側面がエッチングされると共に、Ｐ－ＳｉＮ膜２の開口下端の垂直状態をほぼ維持しながら、上端部が後退し良好なテーパーを形成する。

第１図（ｅ）は上記工程を終えた半導体基板に対して、ホトレジスト４を除去した表面にスパッタリング等により、例えばＡｌ－Ｓｉからなる上層配線５を被着し、開口部に露出した下層配線１との間を電気的接続する。上記工程により、スルーホール部において、ポリイミド膜３の側壁からＰ－ＳｉＮ膜２側壁の上端部にほぼ連続するテーパーを形成することができ、上層配線５の段差被覆性は大幅に改善され、被覆性の極めて優れた上層配線が得られ、極めて安定した接続が得られる。

上記エッチング工程は、コンタクト抵抗，ダメージ等半導体回路素子としての特性に影響することもほとんどないことが確認されている。

また本実施例のエッチング工程は、開口底部では垂直なＰ－ＳｉＮ側壁が形成されるため、微細な開口が形成され、それにもかかわらず段差被覆性の改善が図れ、また同一のリアクティブイオンエッチング装置内で連続的に加工することができ、工程の短縮が図れる。

＜発明の効果＞

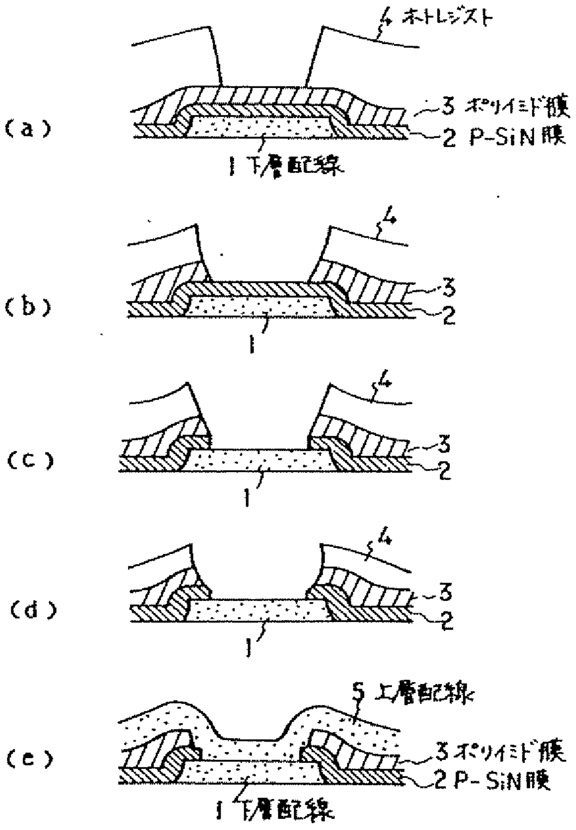
以上のように、本発明によれば、１回のマスク形成により開口部にオーバーハングを生じることなく、側壁に所望のテーパーをつけ、配線材料の段差被覆性を良くし、かつ複合膜を連続的にエッチングすることができる。また複合膜の下層絶縁膜は、異方性エッチングがもつ微細加工を利用していることから、多数の半導体装置（ウエハー）を同時処理した際に、ウエハー間の膜厚等の不均一性によるバラツキを解消するため必要になるオーバーエッチングに対しても、開口部の寸法の拡大が極めて少く、寸法精度の優れた高密度半導体集積回路装置を製造することができる。またエッチング面積の大小、Ｐ－ＳｉＮ膜自身の膜質の変化に強く、再現性の良い開口が得られる。

４．図面の簡単な説明

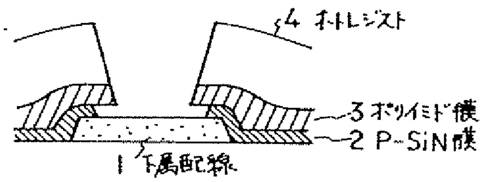
第１図（ａ）乃至（ｅ）は、本発明の実施例を説明するための半導体基板断面図、第２図は、オーバーハングを有する２層絶縁膜の断面図、第３図はオーバーハングをもつ２層絶縁膜に配線材料を被着した半導体断面図、第４図は２層絶縁膜の下層Ｐ－ＳｉＮ膜に異方性エッチングを施した半導体断面図、第５図は２層絶縁膜をもつ半導体のオーバーハング構造を防止するための従来方法を説明する半導体断面図、第６図はエッチングの選択比により開口部のテーパー角を制御した半導体の断面図、第７図乃至第９図は本発明のエッチング条件を導くための測定図である。

１：下層配線　２：Ｐ－ＳｉＮ膜　３：ポリイミド膜　４：マスク材料　５：上層配線

代理人　弁理士　梅田　勝（他２名）



第１図



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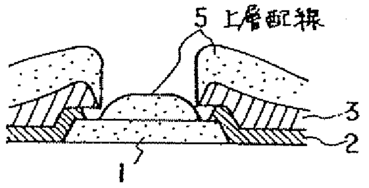

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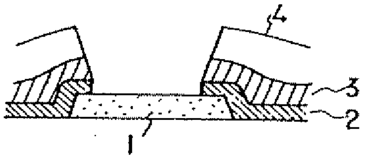

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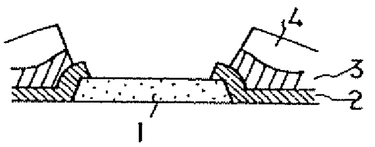

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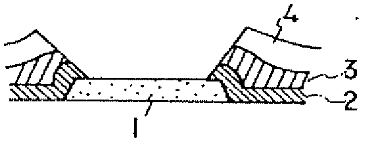

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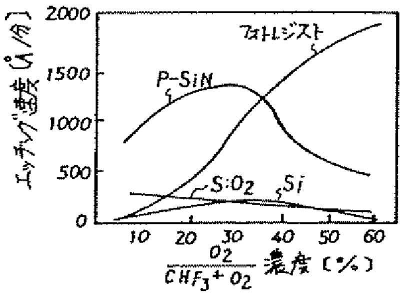
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1000
500
0
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SiO2
Si
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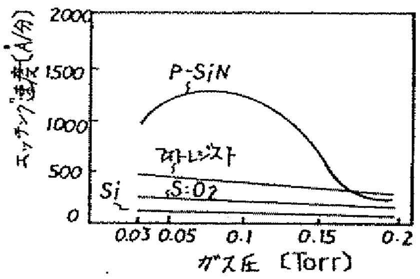
20
30
40
50
60
$\frac{O_2}{CHF_3+O_2}$ 濃度〔%〕

第7図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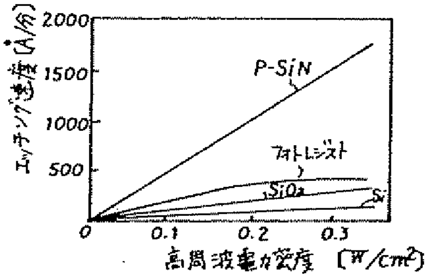
0.2
ガス圧〔Torr〕

第8図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高周波電力密度〔W/cm²〕

第9図

(19) Japan Patent Office (JP)
(12) Publication of Unexamined Patent Application (A)
(11) Japanese Published Patent Application No.: H4-155834
(43) Publication Date: May 28, 1992 (Heisei 4)

(51) Int.Cl.^{5}		Identification Symbol	JPO File No.			
H 01 L	21/3205					
	21/31					
	21/90	M	7353-4M			
			7353-4M	H 01 L	21/88	D
			7342-4M		21/95	

Request for examination: Not made
Number of claims: 2 (5 pages in total)

(54) Title of the Invention: Etching Method for Multilayer Interlayer Insulating Film

(21) Patent Application No.: H2-281469
(22) Patent Application Date: October 18, 1990 (Heisei 2)

(72) Inventor: Masahiko SAITO
c/o Sharp Corporation
22-22 Nagaike-cho, Abeno-ku, Osaka-shi, Osaka-fu
(71) Applicant: Sharp Corporation
22-22 Nagaike-cho, Abeno-ku, Osaka-shi, Osaka-fu
(74) Agents: Patent Attorney, Masaru UMEDA and two others

Specification

1. Title of the Invention

Etching method for multilayer interlayer insulating film

2. Scope of Claims

1) In a method for forming a through hole in an insulating layer electrically separating a multilayer wiring, an etching method for a multilayer interlayer insulating film is characterized in that a through hole is formed by the following steps:

forming a composite insulating film that contains an SiN film and an organic film over a semiconductor substrate on which a lower layer wiring is formed;

forming an aperture in the organic film by dry etching in an atmosphere that contains O_2;

forming an aperture in the SiN film by anisotropic etching in a mixed gas atmosphere that contains CHF_3 and O_2, where the organic film is used as a mask; and

making an aperture wall in the composite insulating film recede in the mixed gas atmosphere that contains CHF_3 and O_2, where the concentration of O_2 is set to be high by conditions for etching of the SiN film.

2) The etching method for a multilayer interlayer insulating film according to Claim 1, wherein the organic film is a polyimide film, and the concentration of O_2 in the CHF_3 and O_2 mixed gas used for anisotropic etching of the polyimide film is set so as to be approximately 10% to 30%.

3. Detailed Description of the Invention

<Field of Industrial Application>

The present invention relates to a manufacturing method for a semiconductor device. In particular, the present invention relates to formation of a through hole that connects an upper layer wiring and a lower layer wiring of a multilayer wiring together.

<Prior Art>

Along with making semiconductor devices more high-density, making electrode wirings be multilayer and making pattern widths finer is being demanded.

In order to respond to this kind of state, formation methods for a multilayer interlayer insulating film are being diversified, as well. For this kind of insulating film, for a process (flattening, making more fine) or device characteristics, a composite layer in which a plurality of various kinds of insulating films are stacked together is often used. For example, for recent devices, a two-layer structure in which a P-SiN film formed by a plasma CVD method and a polyimide film are stacked together is often used for an interlayer insulating film. For main characteristics of this kind of composite film, the following and the like can be given: (1) By use of a P-SiN film as a lower layer, moisture and impurities within a film, due to absorption of moisture by the polyimide film, penetrating into a silicon substrate can be prevented. (2) The number of adverse effects such as surface inversion of the silicon substrate by polarization of the polyimide film and the threshold voltage of a MOS transistor being changed can be reduced. (3) Poor step coverage, formation of cracks, and the like of the P-SiN film are flattened by the upper layer polyimide film, and reliability of the interlayer insulating film can be made even more complete.

For a formation method of a through hole for this kind of stacked-layer composite film, an aperture is formed in the upper layer polyimide film by wet etching (hydrazine solution or alkali developer), dry etching, use of a photosensitive polyimide, or the like.

On the other hand, for the lower layer P-SiN film, an aperture is formed by a dry etching process; however, when etching is performed on the composite film, the polyimide film tends to become an overhang structure with respect to the P-SiN film, in an interface of the polyimide film and the P-SiN film. In FIG. 2, an example of the overhang structure is shown.

In the same drawing, in a P-SiN film 2 and a polyimide film 3 stacked on a lower layer wiring 1, an aperture is formed with a photoresist 4 used as a mask; however, the area of the aperture in the P-SiN film 2 is larger than the area of the aperture in the polyimide film 3, and an overhang structure is formed.

For this kind of case, if an upper layer wiring 5 is deposited over an aperture portion, there are cases where, as shown in FIG. 3, a portion that becomes shaded by the protruded polyimide film 2 is formed, step coverage becomes extremely poor, and disconnect occurs. This problem has been handled in the following ways: as shown in FIG. 4, after the upper layer polyimide film 3 is etched, the lower layer P-SiN film is etched by anisotropic etching; as shown in FIG. 5, in order that the area of the aperture in the P-SiN film 2 of the lower layer be smaller than the area of the aperture in the polyimide film 3 of the upper layer, after an aperture is once formed with a mask material that is deposited over the P-SiN film 2 and the mask material 4 is removed, the polyimide film 2 of the upper layer is deposited thereover and an aperture is formed, and then, either a mask material is formed over each film and etching is performed or, in order to prevent the formation of overhang structure, after the polyimide film 3 and the P-SiN film 2 are etched, etching is performed again on the polyimide film 3 of the upper layer; and, as shown in FIG. 6, the taper angle of the polyimide film 3 of the upper layer is controlled by the taper angle of the mask material 4 and the selection ratio (etch rate ratio) of the mask material 4 and the polyimide film 3, and, furthermore, the taper angle of the P-SiN film of the lower layer is controlled by the taper angle of the polyimide film 3 of the upper layer and the selection ratio of the polyimide film 3 of the upper layer and the P-SiN film 2 of the lower layer, and an aperture that has excellent step coverage is formed by RIE.

<Problems to be Solved by the Invention>

In the aforementioned conventional process, as shown in FIG. 4, in the method in which the P-SiN film 2 is etched by anisotropic etching, even if anisotropy is complete and anisotropy is achieved, due to an increase in the aspect ratio (ratio of the depth to the width of the aperture portion) along with miniaturization in recent years, step coverage of wiring materials becomes poorer.

As shown in FIG. 5, in the method in which forming a mask and etching are performed twice, the steps are complicated, accuracy in alignment whenever a mask is formed is required, and the dimensions of the aperture portion increase. In addition, if there is any misalignment when a mask is formed, cases where the dimensions of the actual aperture portion become too small and cases where electrical conduction becomes unable to be secured occur, as well. Furthermore, in a method for prevention of formation of an overhang structure, where only the polyimide film 3 of the top layer is etched after the aperture is once formed, the P-SiN film 2 of the lower layer is placed in an overhang state. For this reason, there arises a need that the amount of recession by the polyimide film 3 of the upper layer only is adequate, and the dimensions of the aperture increase.

Moreover, as shown in FIG. 6, in the method for controlling the taper angle of an aperture portion by the taper angles of the mask material 4 and the upper layer polyimide film 3 and the selection ratios between the mask material and insulating film and between the insulating films themselves, due to changes in the ratio of the etching area and changes in the film quality of the insulating films themselves, controllability of the taper angle worsens.

Furthermore, because etching is performed with the taper angle being considered from the start, the amount of recession due to overetching increases, and the dimensions of the aperture portion increase. Additionally, up to an optimal amount of etching, even if a good taper is formed, there is a lot of instability, such as that the taper ultimately comes to be in a perpendicular state or the like due to overetching.

The present invention is made in consideration of the problems in the aforementioned conventional method. By the present invention, an etching method by which the level of miniaturization of the dimensions of the aperture and step coverage of the wiring material are made to be adequate is provided.

<Means for Solving the Problems>

In a method for formation of a through hole to connect wirings of an upper layer and a lower layer in a semiconductor device in which a plurality of different kinds of interlayer insulating films are stacked between the wirings of the upper layer and the lower layer, after a polyimide film of the upper layer is etched, a P-SiN film of the lower layer is etched by anisotropic etching with a gas mixture of CHF_3 and O_2, in the gas mixture of CHF_3 and O_2, and under etching conditions that differ from those of the P-SiN film, the wall surface on the aperture side of the polyimide film and the upper edge of the aperture of the P-SiN film are made to recede at the same time, and a through hole that is tapered is formed.

<Embodiment>

FIGS. 1(a) to 1(f [sic]) are cross-sectional-view diagrams of a semiconductor substrate used to describe a first embodiment of the present invention. In particular, steps from a step in which patterning of a mask material is performed after a photoresist is deposited over an insulating film of two stacked layers through an etching step and a step for deposition of wiring materials are shown.

In FIG. 1(a), the P-SiN film 2 is formed over a lower layer wiring 1 by a CVD plasma technique and the polyimide film 3 is subsequently formed thereover to be set as a two-layer composite interlayer insulating film. Next, in order to form an aperture in a desired location in the composite interlayer insulating film, a photoresist 4 is applied over the upper layer insulating film 3, and this is formed into a predetermined pattern. Here, by selection of conditions such as exposure, development, baking, and the like, the taper angle of the photoresist 4 was set to be approximately 80°.

Next, as shown in FIG. 1(b), in order to etch the polyimide film 3 exposed by the aperture portion of the photoresist, first, an aperture is formed in the polyimide film 3 by reactive ion etching (RIE), with O_2 as the main component. Subsequently, as shown in FIG. 1(c), by use of a gas mixture of CHF_3 and O_2, anisotropic etching is performed in a parallel plate dry etching apparatus. Here, for the etching conditions, conditions configured based on the experimental results shown in FIG. 7 to FIG. 9 are implemented. More specifically, for conditions by which the P-SiN film 2 with a perfectly anisotropic shape is obtained, in the gas mixture of CHF_3 and O_2, the mixture fraction of O_2 is set to be from 10% to 30% (FIG. 7), preferably, approximately 20%; the gas pressure is set to be about 0.03 Torr to 0.1 Torr (FIG. 8); and the high frequency power density is set to be greater than or equal to 0.2 w/cm^2 (FIG. 9). By the conditions being set to the aforementioned anisotropic etching conditions, a favorably etched shape with a nearly perpendicular sidewall was obtained. It is to be noted that variations in etching speed depending on the film quality of the P-SiN film 2 can be seen; however, the shape is extremely stable, and it was determined that, after etching was performed, overetching of up to 50% at maximum further took place but no overhang structure was formed, and step management performed at the time of manufacture becomes easy to do.

Subsequently, on a semiconductor substrate on which the P-SiN film 2 was etched to be perfectly anisotropic, as shown in FIG. 1(d), etching was performed again using the gas mixture of CHF_3 and O_2. However, in order that the level of coverage be increased in this step without any detriment to the level of miniaturization, the etching conditions are set to be conditions that differ from those used for the perfect anisotropic etching. That is, etching was performed with the mixture fraction of O_2 at approximately 50% (FIG. 7), the gas pressure at 0.05 Torr (FIG. 8), and the high frequency power density at greater than or equal to 0.2 w/cm^2 (FIG. 9). By performance of etching under the above etching conditions, while side surfaces of the polyimide film 3 are etched and a lower edge of the aperture of the P-SiN film 2 roughly maintains a perpendicular state, the upper edge portion recedes and a good taper is formed.

In FIG. 1(e), with respect to the semiconductor substrate obtained by completion of the above step, over a surface from which the photoresist 4 is removed, for example, the upper layer wiring 5 formed from Al-Si is deposited and electrically connected to the lower layer wiring 1 that is exposed by the aperture portion. By the above step, in a through hole portion, a taper that is nearly continuous from the sidewalls of the polyimide film 3 to the upper edge portion of the sidewalls of the P-SiN film 2 can be formed, step coverage of the upper layer wiring 5 can be dramatically improved, an upper layer wiring that has an extremely superior level of coverage can be acquired, and a extremely stable connection can be obtained.

It was confirmed that there were hardly any effects on contact resistance or effects such as damage and the like on the characteristics of a semiconductor circuit element by the above etching step.

In addition, because a perpendicular side wall of the P-SiN film is formed at the base of the aperture by the etching steps of the present embodiment, a minute aperture can be formed, and despite the fact that the aperture is minute, an improvement in step coverage can be obtained, and further, processing can be performed consecutively in the same reactive ion etching apparatus, and a reduction in the number of steps can be obtained.

<Advantageous Effects of the Invention>

As described above, by the present invention, by a one-time formation of a mask, a desired taper can be attached to a sidewall, step coverage of a wiring material can be improved, and continuous etching of a composite film can be performed with no generation of overhang in the aperture portion. Furthermore, because microfabrication in anisotropic etching is used for the lower layer insulating film of the composite film, even with overetching, which is needed to eliminate variations due to non-uniformity in film quality and the like between wafers whenever a number of semiconductor devices (wafers) are processed simultaneously, the amount of increase in the dimensions of the aperture portion is extremely small, and a high density semiconductor integrated circuit can be manufactured. Furthermore, an aperture that is resistant to changes in the size of the etching area and changes in the film quality of the P-SiN film itself and that has a high level of reproducibility can be obtained.

4. Brief Description of the Drawings

FIGS. 1(a) to 1(e) are cross-sectional-view drawings of a semiconductor substrate used to describe an embodiment of the present invention. FIG. 2 is a cross-sectional-view drawing of a two-layer insulating film that has overhang. FIG. 3 is a cross-sectional-view drawing of a semiconductor in which a wiring material is deposited over the two-layer insulating film that has overhang. FIG. 4 is a cross-sectional-view drawing of a semiconductor in which anisotropic etching is performed on a P-SiN film that is a lower layer of the two-layer insulating film. FIG. 5 is a cross-sectional-view drawing of a semiconductor used to explain a conventional method for prevention of an overhang structure of a semiconductor that includes the two-layer insulating film. FIG. 6 is a cross-sectional-view drawing of a semiconductor in which a taper angle of an aperture portion is controlled by the selection ratio of an etching process. Each of FIG. 7 to FIG. 9 is a measurement graph used as a guide for etching conditions of the present invention.

1: lower layer wiring, 2: P-SiN film, 3: polyimide film, 4: mask material, and 5: upper layer wiring.

Agent: Patent Attorney, Masaru UMEDA (and two others).